Amendments to the Claims

Listing of Claims:

1. (previously presented) A phase locked loop (PLL) generating a phase locked signal and adjusting a frequency of the phase locked signal according to an incoming signal having periodic frames, the PLL comprising:

an oscillator for generating the phased locked signal; and

a frequency detection module electrically coupled to the oscillator for detecting two regular patterns within two different frames of the incoming signal, calculating a number of periods of the phase locked signal corresponding to a distance between the two regular patterns, and controlling the oscillator to adjust the frequency of the phase locked loop signal according to the number of periods.

2. (original) The PLL of claim 1, wherein the frequency detection module comprises:

a pattern detector for detecting the two regular patterns in the incoming signal;

a counter electrically coupled to the pattern detector for calculating the number of periods of the phase locked signal corresponding to the distance between the two regular patterns; and

a comparator electrically coupled to the counter for comparing the number of periods with a predetermined value to generate a control signal, and using the control signal to control the oscillator to adjust the frequency of the phase locked signal.

3. (original) The PLL of claim 2, wherein if the number of periods is less than the predetermined value, the comparator uses the control signal to control the oscillator to increase the frequency of the phase locked signal; and if the number of periods is greater than the predetermined value, the comparator uses the control signal to control the oscillator to decrease the frequency of the phase locked signal.

4. (original) The PLL of claim 2, wherein the frequency detection module further comprises a control interface electrically coupled to the comparator for controlling the oscillator to adjust the frequency of the phase locked signal according to the control signal.

5. (original) The PLL of claim 1, wherein the incoming signal is a modulation signal and the two regular patterns are sync patterns of the modulation signal.

6. (currently amended) The PLL of claim 1, wherein the oscillator is ~~a voltage controlled oscillator,~~ a numerical controlled oscillator[[,]] or a current controlled oscillator.

7. (original) A method for producing a phase locked signal and adjusting a frequency of the phase locked signal according to an incoming signal, the method comprising the following steps:

(a) producing the phase locked signal;

(b) detecting two regular patterns in the incoming signal;

(c) calculating a number of periods of the phase locked signal corresponding to a distance between the two regular patterns; and

(d) adjusting the frequency of the phase locked signal according to the number of periods.

8. (original) The method of claim 7, wherein step (d) comprises comparing the number of periods with a predetermined value, and adjusting the frequency of the phase locked signal according to a result of the comparison.

9. (original) The method of claim 8, wherein step (d) further comprises if the number of periods is less than the predetermined value, increasing the frequency of the phase locked signal; and if the number of periods is greater than the predetermined value, decreasing the frequency of the phase locked signal.

10. (original) The method of claim 7, wherein the incoming signal is a modulation signal and the two regular patterns are sync patterns of the modulation signal.

11. (previously presented) The PLL of claim 1 further comprising:

a frequency detector for calculating a difference in frequency between the incoming signal and the phase locked loop signal, and further for controlling the oscillator to adjust the frequency of the phase locked loop signal according to the difference in frequency; and

a multiplexor coupled to the frequency detector, the frequency detection module, and the oscillator, the multiplexor for selecting one of the frequency detector or the frequency detection module to control the oscillator to adjust the frequency of the phase locked loop signal;

wherein the multiplexor first selects the frequency detector to control the oscillator to adjust the frequency of the phase locked loop signal, and then selects the frequency detection module to control the oscillator to adjust the frequency of the phase locked loop signal if the PLL has not entered into a locked state after a predetermined time.

12. (New) The PLL of claim 1 wherein the two different frames are non-adjacent frames.

13. (New) The method of claim 7 wherein the two regular patterns are within two non-adjacent frames.